ROSTEC Engineering
Phone +45 3967 6438 Fax +45 3966 6438 Website www.rostec.dk E-mail rostec@rostec.dk

CAD324 Clock and AES3id Distribution Amplifier

ROSTEC CAD324 Clock and AES3id Distribution Amplifier

Revision 4, December 26, 2009

CAD324 Clock and AES3id Distribution Amplifier

Contents

CAD324 Clock and AES3id Distribution Amplifier

Features

- 3 inputs into 24 outputs (3 groups of 8).
- Distributes word clocks from 1 Hz to 25 MHz.
- Converts sine waves to square waves.
- Distributes AES3id with sample rates ranging from 8 kHz to 768 kHz.
- Extracts word clock from SPDIF/AES3id/AES3 at sample rates from 8 kHz to 192 kHz.
- Balanced inputs for ground noise cancellation.
- The Inputs have "sweet spot" detectors, providing auto-slicing and signal clean-up.
- Inputs accept from 0.2 Volts to 10 Volts.
- Individual selectable output level for each output group. Choose between TTL for word clocks or bipolar for AES3id.
- Ultra high speed long haul output buffers.
- 75 ohms output via BNC connectors.
- Latency from input to output is 30 nsec
- Separate power supplies for inputs and for each output group.
- Linear low noise power supplies.
- Short circuit proof. Self protecting. Individual thermal protecting for each output group.
- Inputs and outputs are ESD protected to 23 kV, IEC 61000-4-2 and 15 A surge, IEC 61000-4-5
- 19" sturdy steel metal casing
- Affordable price

General description

The CAD324 is a high quality distribution amplifier designed to operate in a broadcast, video or audio studio installation. It distributes clocks and AES3id with the correct output levels and output formats.

It has 3 inputs and 24 outputs configured as 3 groups of 8 outputs. Any of the 3 output groups can be freely selected to connect to any of the 3 inputs. The inputs accept clocks from 0.2 Volts to 10 Volts, SPDIF, AES3id and AES3 (11) levels.

It has an overall bandwidth of 40 MHz, which makes it able to distribute all the standard clocks, from 1Hz **(*)** to 24.576 MHz. This means that all standard audio clocks, Telecom clocks and GPS clocks are within its operating range.
Further, it is able to convert the sine wave output from a standard GPS receiver into a TTL square wave.

It distributes AES3id with sample rates from 8 kHz to 768 kHz, and it is able to extract the word clock signal from an incoming SPDIF, AES3id or AES3 (11), as long as the sample rate is within the range of 8 kHz to 192 kHz.
The word clock extraction is performed by hardware logic directly on the AES signal. The reason is to avoid the poor jitter performance of standard AES receivers. This method introduces the least possible jitter - in the order of a few picoseconds.

The input and output circuits are state of the art, resulting in an impressive 40 MHz overall bandwidth. The latency from input to output is approx. 30 nsec.

The input circuit and each of the 3 output groups have their own individual power supply. The separate power supplies and separate internal ground planes creates an efficient isolation barrier between groups, eliminating crosstalk and jitter transfer when different sampling frequencies and different data structures are distributed through the same unit.

Each of the inputs features a discrete high-speed comparator with hysteresis and a "sweet spot" detector, which performs an accurate auto-slicing of the input. This means that the circuit automatically chooses the most useful part of the input signal, thus being able to clean-up and reconstruct a ringing and noisy input signal into a perfect output signal.

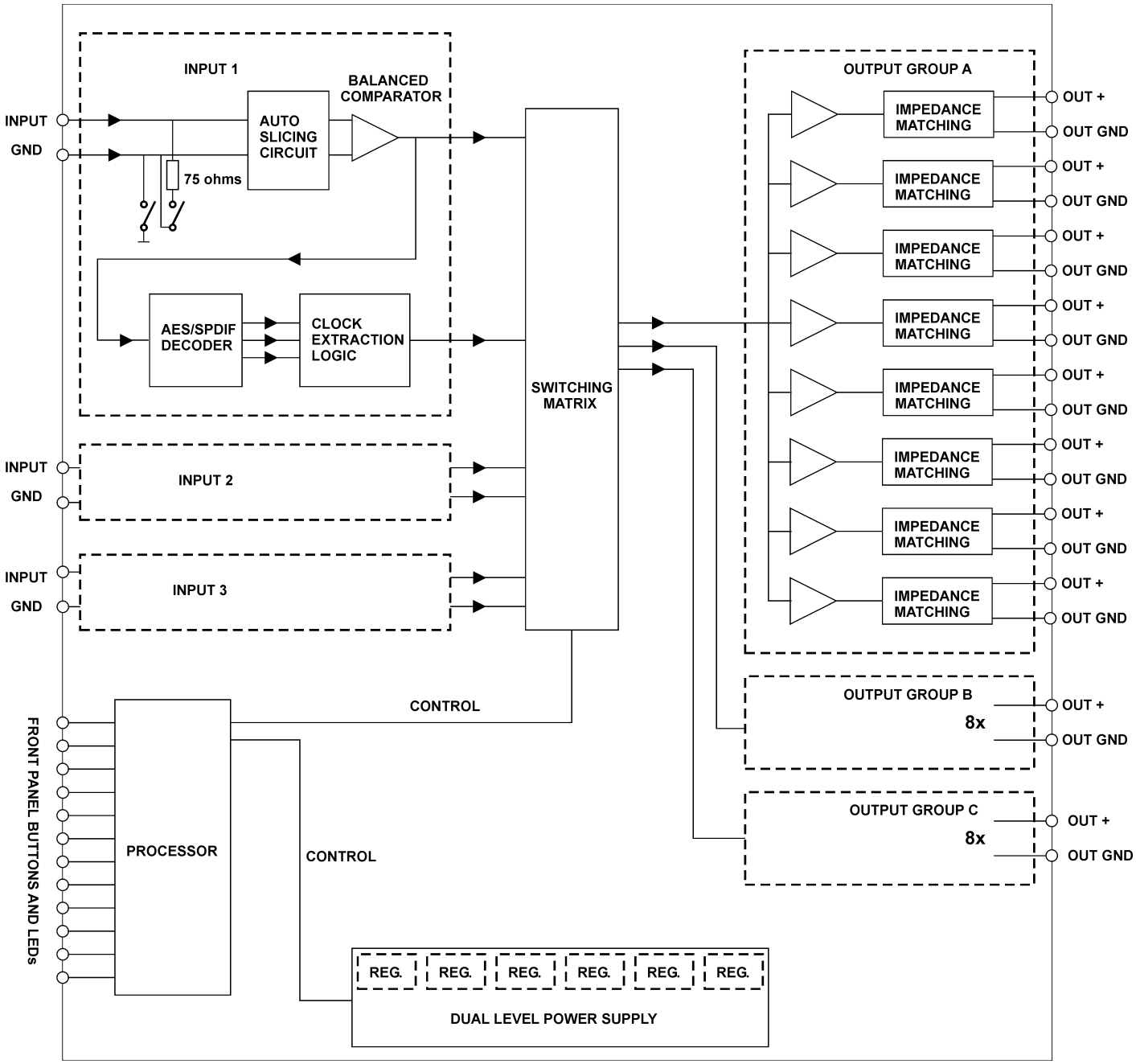
The 24 individual output buffers are ultra high speed with accurate output impedances, making them well suited for long haul. The output levels of each individual group can be selected by push buttons on the front: 75 ohms TTL compatible for word clocks, and 75 ohms bipolar for AES3id. The maximum AES3id level that is allowed by the AES standard is applied in order to minimize noise pick-up in the cabling.

The output buffers are fast! The rise time of the output pulse is less than 3 nsec into 75 ohms with an overshoot/undershoot of less than 5%.
The fast rise time makes the output signal appear well defined and clear cut seen from a receiver's point of view. This enables the receiver to react to the signal with maximum accuracy and minimal jitter.

(*) at *1 Hz the input level must be TTL level.*
.

CAD324 Clock and AES3id Distribution Amplifier

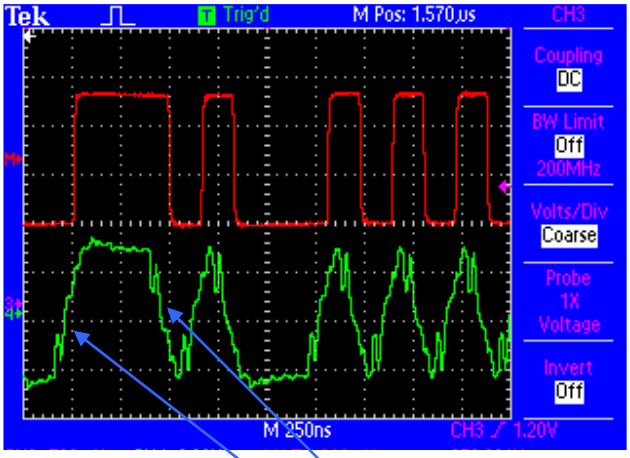
Simplified Functional Schematic



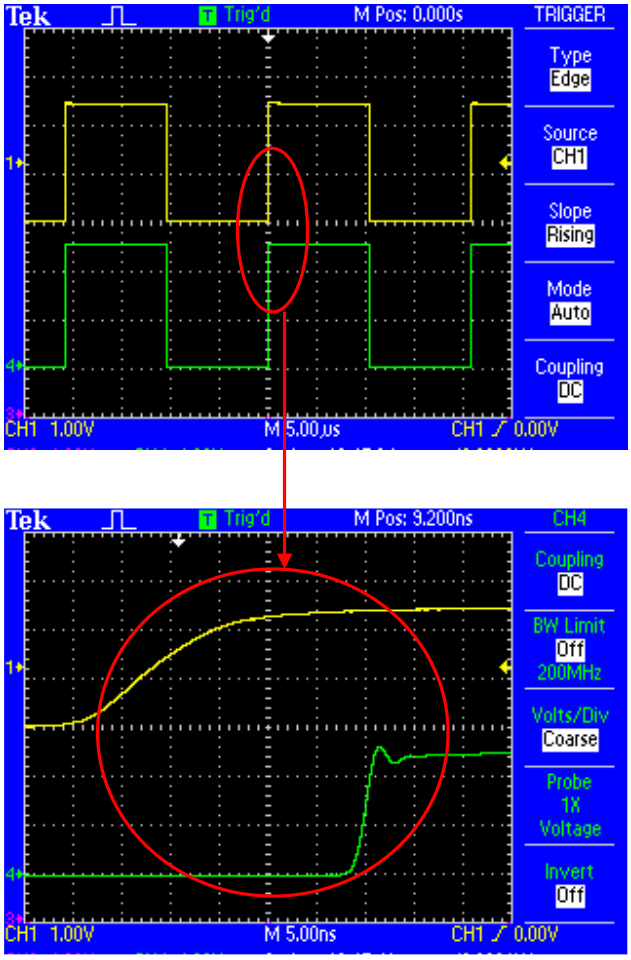
Input circuit

Each input circuit consists of a discrete balanced high speed comparator. The signal from the input connector is fed balanced into the comparator, in order to reject any common mode noise and spikes that are created as common mode noise in the cabling. This configuration is able to establish the trigger point at the incoming signal with great accuracy, with a dramatically improved jitter response as a result.
The input circuit also features a "sweet spot" detector, which detects ringing and HF noise and performs auto slicing, automatically placing the trigger point inside the healthiest window of the input signal.

The mechanism is able to regenerate a wildly distorted input signal into a clear-cut perfect output signal.
The oscilloscope snapshot below illustrates this clearly. The lower trace is an AES at 48 kHz input signal with lots of noise and ringing, due to some wrong termination, incorrect cable impedance or faulty grounding.
The upper trace is the reconstructed signal measured at the output.



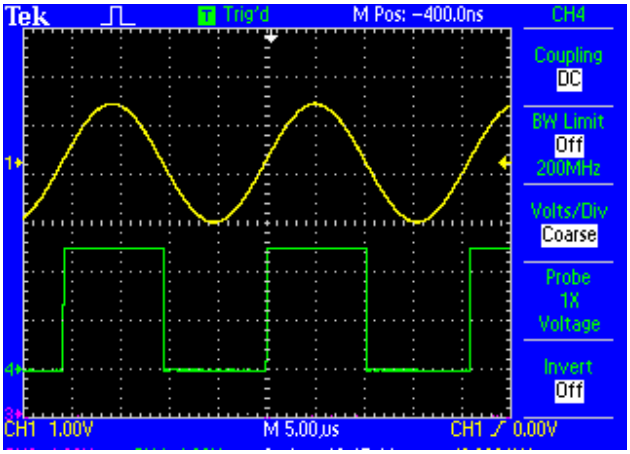
The next scope snapshot is a 48 kHz input clock and the resulting output clock. The upper trace is the input; the lower trace is the output.
Not much to say about it, except that the input is reproduced faithfully at the output. But a closer look reveals some interesting details.



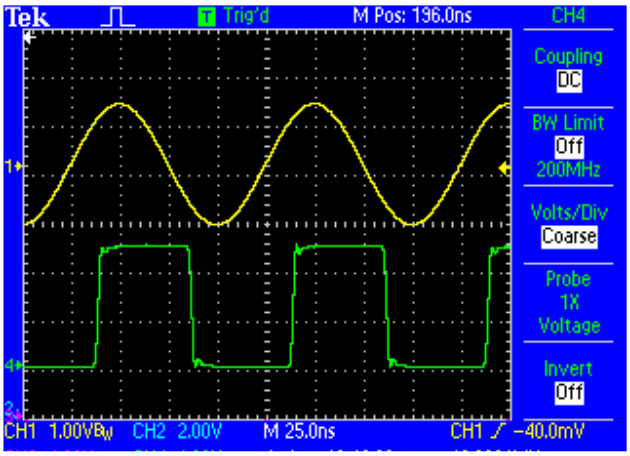
It can be seen from the magnification that the time delay (latency) of the unit is approx. 25 nsec when it is running in clock mode. Also, there is some cable ringing of approx 5%. The measurement was made with 10 m standard 68pF/m cable, terminated with 75 ohms.

The next two scope snapshots show the sine to square wave converting characteristics of the CAD324.
The first snapshot shows a 48 kHz sine wave converted into a TTL square wave output
A sine wave was used because it represents the slowest rise time at a given frequency, i.e. the signal stays the longest time in the trigger zone. Hence it represents the greatest challenge for the input comparator circuit.

CAD324 Clock and AES3id Distribution Amplifier



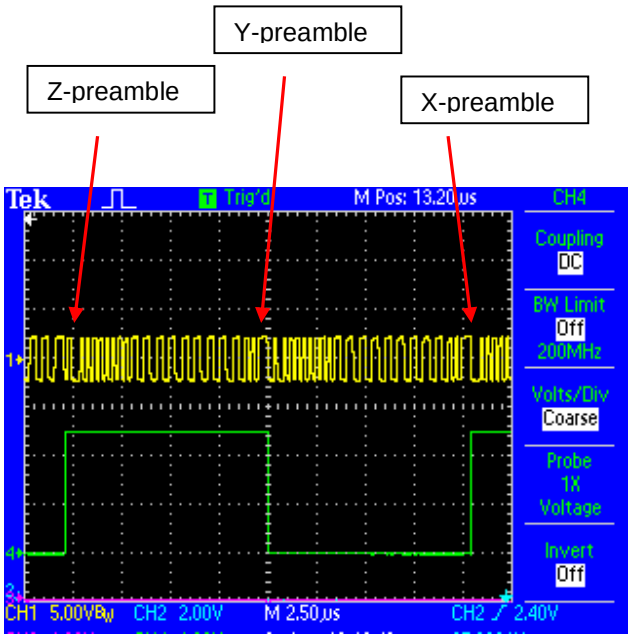
This snapshot shows a 10 MHz sine wave from a typical GPS receiver, converted into a TTL square wave.



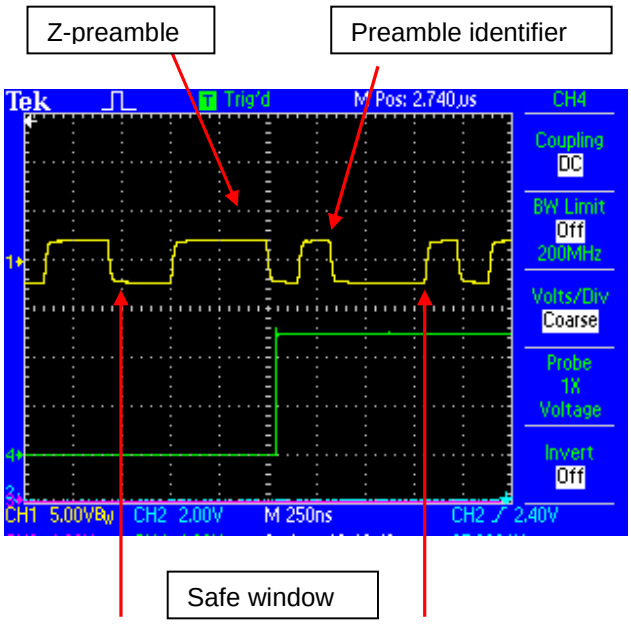
Clock extraction from the AES data stream

The CAD324 is able to extract the word clock from an AES3, AES3id or SPDIF data stream. The mechanism is based on pure hardware logic circuitry, as opposed to a PLL based AES receiver.
The reason is jitter performance. Manufacturers of AES receivers like to claim impressive jitter specs, some of them down to 50 psec or better, but in reality they are closer to 3 nsec PP measured at the word clock. This fact is cleverly concealed by the various manufacturers, by specifying jitter as measured between consecutive leading edges of the recovered master clock.
Shame on them!

Below is seen how the CAD324 extracts the word clock from the AES data stream



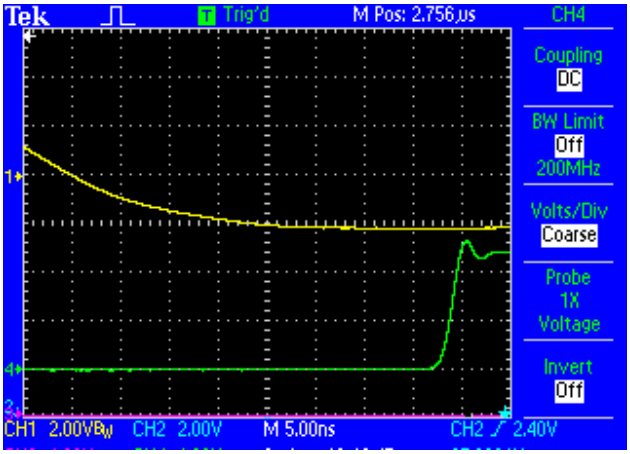
The extraction is done in the middle of the "safe window" where a clear definition exists between which audio data belongs to the low part of the word clock, and which audio data belongs to the high part of the word clock.



The hardware clock extraction method yields excellent jitter specifications. The extraction is performed right at the trailing edge of the extended pulse in the preamble, safely away from all audio data and channel status data. This position is the ultimately quiet point in the AES data stream.

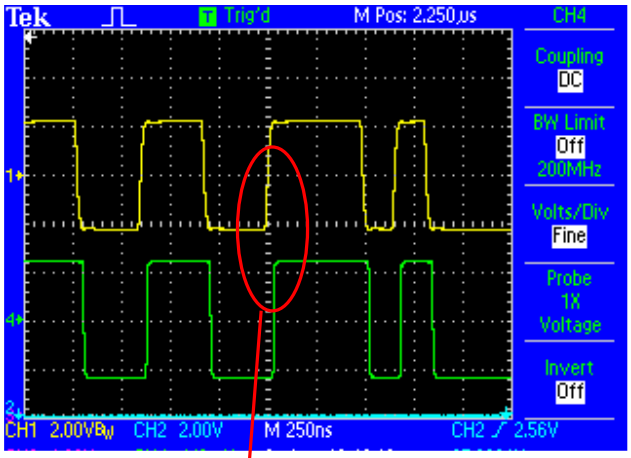
An expanded view of the relationship between the AES data stream and the extracted word clock shows the jitter performance.
The upper trace is the AES from a clean source, like the ROSTEC ASD16HD reference generator.
The lower trace is the extracted word clock at the output of the CAD324.
The time scale is 5 nsec/div

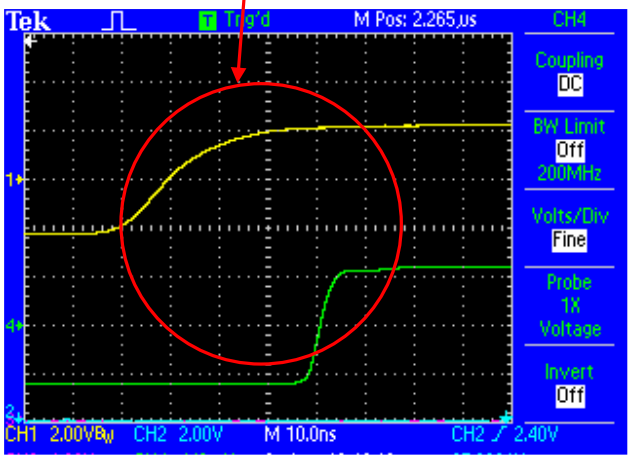
- Jitter? What jitter?



AES3id mode

Below is a snapshot of an AES3id input and the resulting AES3id output.
The upper trace is an AES3id at 48 kHz sample rate.
The lower trace is the AES3id output.
The output is 1.2 Volts into 75 ohms, as is described in the AES recommendation. Also note that the output is bipolar as it is recommended.





A closer look at the area of interest shows that the time delay (latency) is slightly longer in AES3id mode than in TTL mode, i.e. 30 nsec versus 25 nsec.
The overshoot is optimized in AES3id mode, with a slight penalty in bandwidth. The rise time is 5 nsec in AES3id mode, as opposed to 3 nsec in TTL (clock) mode.

Switching matrix

The switching system is just a cross-point switch, connecting the inputs to the outputs according to the settings on the front panel.
The switch is controlled by the system microprocessor, and the settings are saved immediately in non-volatile memory when changes are made on the front panel.
It is instant memory!

Power supply

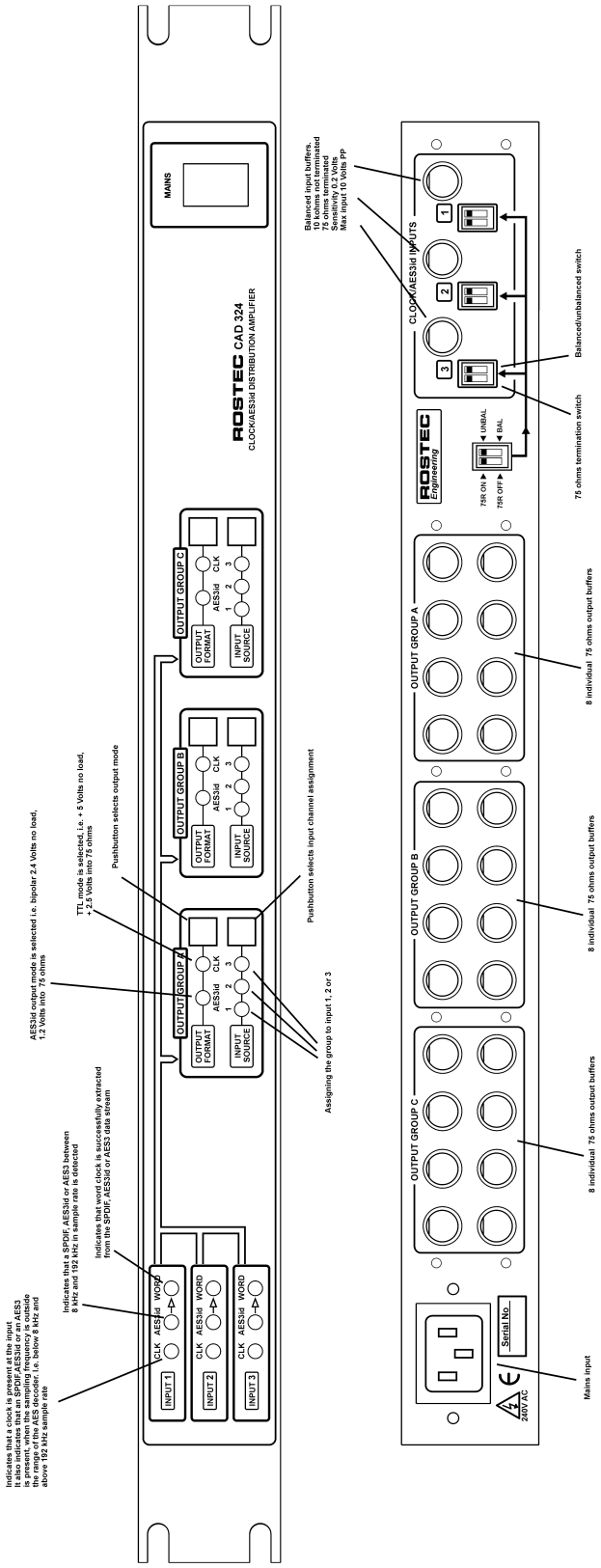
The unit has 4 separate power supplies. One for the input section and one for each of the output groups. Each group has separate ground planes as well as separate ground wiring.
This architecture ensures that ground currents and supply transients cannot cross between the groups.

This configuration is essential for low jitter specifications. When different sampling frequencies and different data structures are distributed via the 3 output groups, crosstalk will invariably create data jitter. .
The independent power supplies and the separate ground planes together with the advanced signal architecture have efficiently eliminated this problem.

To further maintain the excellent jitter and low noise specifications, the unit is equipped with a toroidal mains transformer and a high quality mains input filter.

CAD324 Clock and AES3id Distribution Amplifier

Front and back panel quick guide



CAD324 Clock and AES3id Distribution Amplifier

Mechanical and electrical specifications:

Dimensions	: Width 19 inch, height 1U (44 mm), depth 150 mm
Weight	: 3.0 kg
Power	: 180 - 240 VAC 50 Hz, 8 Watts (EU Version)
	: 90 -120 VAC 60 Hz, 8 Watts (US Version)
Inputs	: Number of: 3
	: Balanced, 10 kohms no termination, 75 ohms terminated,
	: Sensitivity 0.2 Volts PP, maximum 10 Volts PP
	: Compatible with AES3 (11), AES3id and S/PDIF levels
	: ESD protected to 23 kV, IEC 61000-4-2 and 15 A surge, IEC 61000-4-5
Outputs	: Number of: 24
	: Configuration: 3 groups of 8 outputs each. Individual buffers.
	: TTL output mode: + 5 volts no load, + 2.5 Volts into 75 ohms
	: AES3id mode: 2.4 Volts bipolar no load, 1.2 Volts bipolar into 75 ohms
	: ESD protected to 23 kV, IEC 61000-4-2 and 15 A surge, IEC 61000-4-5
Environment	: 0 - +50 deg C operating
	: 0 - +70 deg C storage