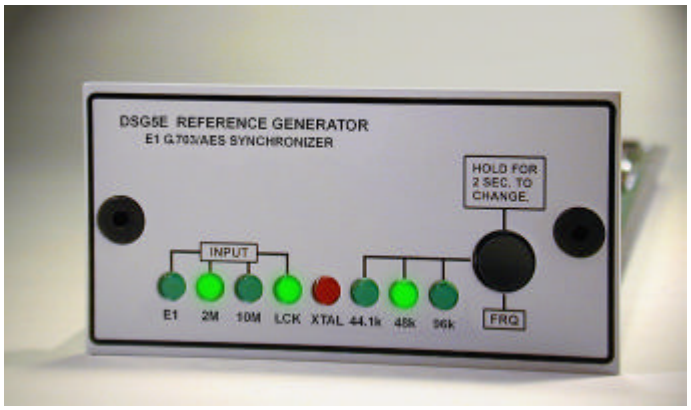
ROSTEC Engineering
Christianehøj 43, 2860 Søborg, Denmark
Phone +45 3967 6438 Fax +45 3966 6438 E-mail rostec@post6.tele.dk Website www.rostec.com



ROSTEC DSG5E

Reference Generator/ E1 G.703 Synchronizer for GPU frame

General description

The DSG5E is a GRADE1 crystal controlled Digital Audio Reference Generator with AES11 and SDIF-2 Word outputs.
It is able to lock on to an AMI (Alternate Mark Inversion) coded 2Mbit E1 CCITT G.703 signal, a 2.048 MHz clock from E1 interfaces or a 10 MHz clock from GPS receivers.
It is based upon an extensive sync safety philosophy, guarding efficiently against sync dropouts by means of a built in flywheel and a unique glide principle.
When an external reference is applied, the generator will slide gently into lock without any jumps or interruptions of the output sync signals.
When the external reference is momentarily absent or lost the generator will immediately switch to internal flywheel mode, keeping the sync position and frequency inside narrow limits. When the external reference returns, the oscillator will slowly correct for the accumulated drift in time of its internal crystal oscillator, gently bringing the outputs back into perfect sync.
When the generator operates in flywheel mode, the flywheel inertia will gradually be exhausted and will eventually expire after a maximum of 80 seconds. If the incoming reference is not reestablished before this happens, the control is handed over to the internal crystal reference, which is of AES GRADE1 precision. This scheme ensures a continuous synchronization of the connected equipment, even when large dropouts of the incoming sync signal are to be expected.

A two-step process performs jitter and wandering attenuation. First, a crystal oscillator based jitter attenuator operates directly on the clock recovery circuit of the E1 line receiver interface. Second, the recovered clock is routed to the main phase locked loop circuit, which exhibits an excellent Jitter Rejection Ratio (se curve on page 3).
The result is an impressive ability to clean up and stabilize an unstable or jittery house sync.
The E1 G.703 line receiver has a jitter tolerance exceeding the requirements of Publications 43802, 43801, 62411 amended, TR-TSY-000170 and CCITT REC G.823
When more than one input source is connected, the DSG5E generator automatically selects the active input by priority.1: E1 G.703, 2: 2.048 MHz. 3: 10 MHz, 4: Internal crystal

Powering up

There are no special considerations to observe when powering up the unit. When an external reference is connected upon power up, the generator will reset itself as close as possible to the relevant sync position, and it will immediately be able to achieve lock, as long as the incoming

reference is better than +/-30 ppm in absolute frequency precision.

E1 G.703 input

The 2Mbit E1 CCIT G703 input has a transformer balanced E1 line receiver interface, the input transformer being center-grounded on the IC side and floating on the line input side. The circuit performs a dynamic establishing of thresholds, clock recovery and jitter attenuation by means of a local crystal controlled reference clock, able to phase lock to the recovered clock.
This scheme dramatically reduces incoming jitter, creating an input jitter tolerance very close to the theoretically possible, which is 0,46UI equal to approx. 112nSec. The input jitter tolerance exceeds the requirements of Publications 43802, 43801, 62411 amended, TR-TSY-000170 and CCITT REC G.823
The recovered clock is evaluated for errors and continuity for 2 seconds, after which it is routed to the main phase comparator circuit for use as a frequency reference for the AES/word outputs.
Loss of signal is detected upon receiving 175 consecutive zeroes, after which frequency control immediately is handed over to the main flywheel circuit.
The signal is accepted again when ones density reaches 12,5%, based on 175 bits periods with less than 100 consecutive zeroes, as prescribed in ANSI T1.231-1993.

2.048 MHz input cct

The 2.048 MHz input is intended for recovered or transmitted system clocks in E1 applications. There is no position information in 2.048 MHz signal, so the correct mathematically relationship between incoming and outgoing word/AES sampling frequency is calculated, and a phase lock is performed on the result.
When the input is lost and reestablished, the generator simply grabs the first available leading edge of the 2.048 MHz signal, makes the correct calculation and performs the phase lock.
The circuit evaluates the incoming signal for errors and continuity for 1 second before it locks on to it.
The total lock time is approximately 3 seconds and the maximum time shift between input and output during the lock on sequence is 500 nSec. This is equal to an output frequency correction of less than 1 ppm.

10 MHz input cct

The 10 MHz input is in principle identical to the 2.048 MHz input, but the lock mechanism is slightly faster
The total lock time is approximately 2 seconds and the maximum time shift between input and output during the lock on sequence is 200 nSec. This is equal to an output frequency correction of less than 1 ppm.

Word output

There are two individually buffered Word outputs, 75 ohm, TTL level.

AES output

There are two individually buffered transformer balanced AES outputs, 110 ohms RS422 as prescribed in the AES/EBU standards for professional/broadcast equipment.

No Sync alarm

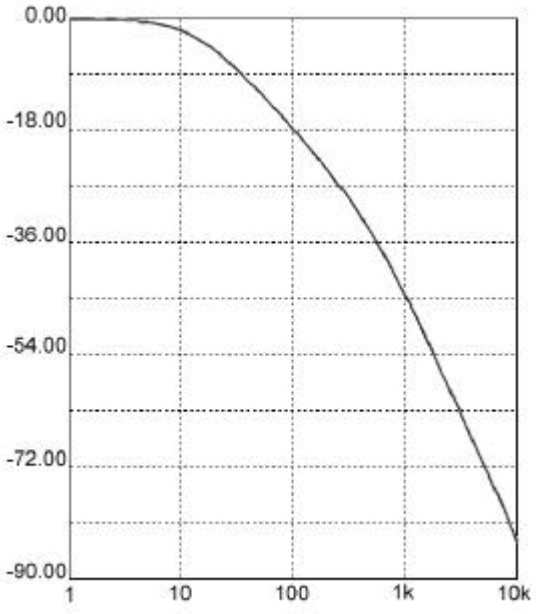
The alarm output is TTL level, 1 kohm. It is high when lock to external reference is established. It changes state to low when sync is lost.

Ability to reject jitter

The jitter presented at the inputs will not directly be transferred to the outputs. It will be greatly reduced and in most situations almost total eliminated.
The curve illustrates the excellent Jitter Rejection Ratio of the DSG5E. The corner frequency of the jitter rejection curve is approx. 12 Hz for the first pole and 500 Hz for the second pole.
In the frequency band above 700 Hz, where jitter can create problems in standard A/D and D/A

Christianehøj 43, 2860 Søborg, Denmark
Phone +45 3967 6438 Fax +45 3966 6438 E-mail rostec@post6.tele.dk Website www.rostec.com

converters, the output jitter is reduced to residual HCMOS buffer noise, even when an extreme jitter level is present at the input.



Jitter Attenuation dB vs. Frequency.
E1 G.703 Input to AES output

Additional Technical Information

General

The DSG5E has a straight forward, but powerful architecture. The input reference is automatically selected by priority from left to right on the front panel and fed to the sync input circuit. When an input signal is present, the circuit calculates the mathematical relationship between input and output clocks and generates a common denominator, which is used as a basis for the phase lock mechanism.
Note that the frequencies 2.048 MHz, 10 MHz, 44.1 kHz, 48 KHz and 96 kHz do not have a simple relationship. Thus looking at the input and output of the generator with an oscilloscope will reveal a picture where one signal seem to be "running" with respect to the other, although the LOCK LED indicates a phase lock.
In order to get a steady picture, a trigger point for the scope is available on the PCB (TP1, common denominator).

Flywheel cct

When the input is lost, an internal flywheel circuit immediately takes over, keeping the input and output frequencies inside narrow limits, typically less than 0.1 ppm. When the input returns, the generator slowly corrects for the accumulated drift, gently bringing the input and output back into perfect sync.
When operating in flywheel mode, the flywheel inertia will gradually be exhausted and it will eventually expire. There are jumper settings for 5, 10, 20, 40 and 80 seconds.
If the input is not reestablished before timeout, clock control is handed over to the internal crystal reference, which has a frequency accuracy of better than 1 ppm.
Operation of the flywheel circuit is identical in all input modes.

44.1kHz/48kHz/96 kHz sampling frequency

The AES/Word generator output sampling frequency is selected by a pushbutton that toggles between the available frequencies. The pushbutton has a 2 seconds time delay to protect against accidental change.
Sampling frequency at power up can be set by internal wiring to 44.1 kHz, 48 kHz or 96 kHz. Factory default is 48 kHz

Word Outputs

The Word outputs are available on the standard SUB-D connector on the back panel. The outputs are individually buffered, 75 ohms and TTL level. The word output frequency follows the chosen sampling frequency on the front panel, i.e. 44,1 kHz, 48 kHz or 96 kHz.

Christianehøj 43, 2860 Søborg, Denmark
Phone +45 3967 6438 Fax +45 3966 6438 E-mail rostec@post6.tele.dk Website www.rostec.com

The rising edge of the word is aligned to the AES subframe A and the trailing edge is aligned to the subframe B. Thus a high level indicates left channel and a low level indicates right channel of the audio data.

AES outputs

The AES outputs are available on the SUB-D connector on the back panel. The outputs are individually buffered, 110 ohms, transformer balanced and 4V PP when terminated.
The AES signal is intended for synchronization purposes and should normally be empty of audio data, i.e. all audio data bits are set to zero. This would minimize the build-up of jitter in cables, as the format would then produce a biphase coded AES signal with a large portion of the frame having identical pulses.
However, some commercially available AES receiver chips exhibits PLL lock problems when subjected to a "black" AES signal, producing an unstable and jittery master clock.

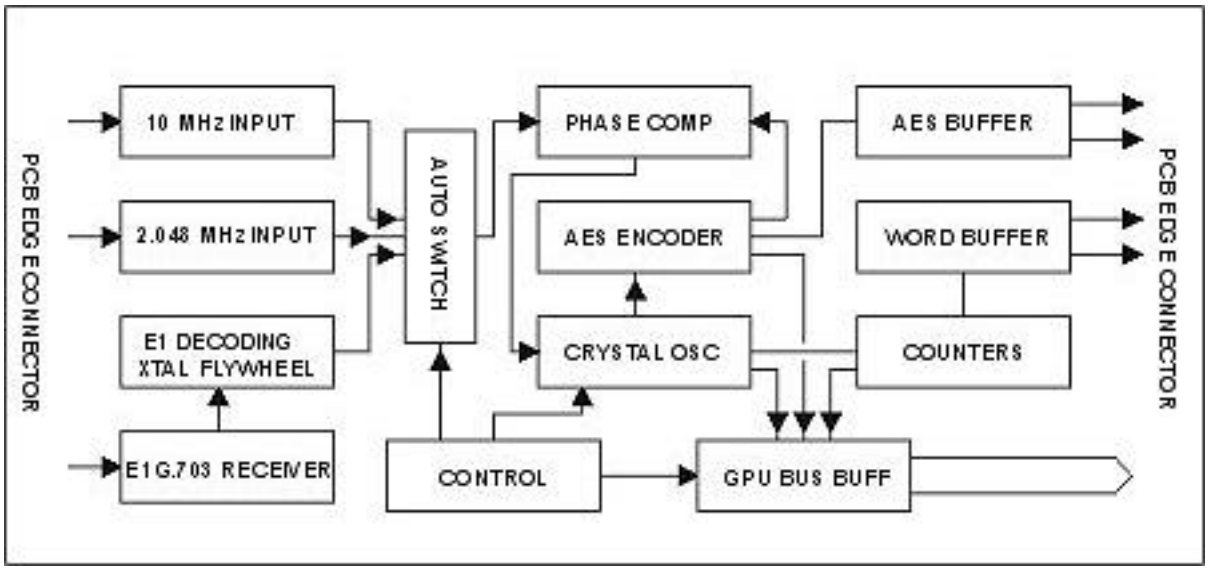
The problem has been overcome by setting the first eight audio data bits to 1, and the remaining sixteen bits to 0. This gives a DC offset in the audio signal of –90 dBFS or approximately 0.2 mV with reference to +18 dBu.
A standard digital audio input circuit will easily accommodate this DC offset, and the scheme efficiently eliminates the AES receiver lock problems.

GPU Bus outputs

The Generator outputs all relevant clocks and control signals on a 10-bit GPU bus connecting all modules in the GPU frame.
The signals are used to control and synchronize digital output modules, such as Analog/Digital and Sample Rate Converters, in order to ensure correct synchronization of all digital outputs.
The GPU bus also performs reset requests, out of sync monitoring and direct communication with the BBG3 Video Generator and the Word or AES distribution amplifiers.

ROSTEC Engineering
Christianehøj 43, 2860 Søborg, Denmark
Phone +45 3967 6438 Fax +45 3966 6438 E-mail rostec@post6.tele.dk Website www.rostec.com

Block Schematic:



Electrical specifications:

Reference Inputs : E1 CCITT G.703 , Transformer balanced 75ohm,
Nom. level (0 dB) 2,4V PP, Sensitivity 13,6 dB below 0 dB
: 2.048 MHz clock 10 kohms, TTL Level
: 10 MHz clock, 10 kohms, TTL level

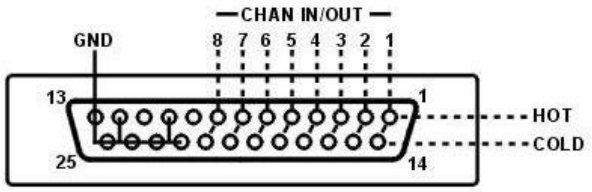
Outputs : 2 x AES11 transformer balanced 110 ohms RS422
: 2 x SDIF-2 word clock, 75 ohm, TTL level
: No-sync alarm 1 kohm TTL level

Stability/accuracy : Oven Crystal accuracy 0,5 ppm/25 deg. C, stability 0.5 ppm 0 - 50 deg. C
: PLL capture range max. +/-50 ppm.
: PLL jitter < 1 nsec SS, 700Hz - 100kHz

ROSTEC Engineering
Christianehøj 43, 2860 Søborg, Denmark
Phone +45 3967 6438 Fax +45 3966 6438 E-mail rostec@post6.tele.dk Website www.rostec.com

IN/OUT CONNECTIONS DSG5E

25 POLE SUB-D FEMALE CONNECTOR AT THE GPU BACK PANEL



E1 G.703 Input: Hot pin1, Cold pin14
2.048 MHz Input: Hot pin2, Gnd pin15
10 MHz Input: Hot pin3, Gnd pin16
No Sync alarm: Hot pin4, Gnd pin24
Word Output 1: Hot pin5, Gnd pin18
Word Output 2: Hot pin6, Gnd pin19
AES Output 1: Hot pin7, Cold pin20, Gnd pin22
AES Output 2: Hot pin8, Cold pin21, Gnd pin 23