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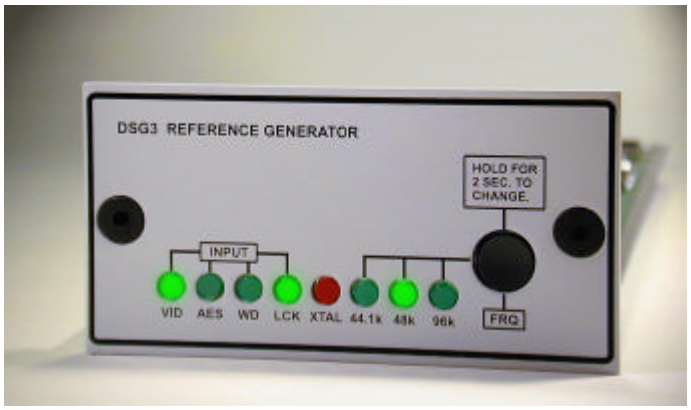

ROSTEC DSG3 Digital Reference Generator for GPU frame

General description

The DSG3 is a crystal controlled Digital Audio Reference Generator with AES11 and SDIF-2 Word outputs.
It is able to lock on to standard PAL/CCIR or SECAM video, SDIF-2 Word or AES/EBU.
It is based upon an extensive sync safety philosophy, guarding efficiently against sync dropouts by means of a built in flywheel and a unique glide principle.
When an external reference is applied, the generator will slide gently into lock without any jumps or interruptions of the output sync signals.
When the external reference is momentarily absent or lost the generator will immediately switch to internal flywheel mode, keeping the sync position and frequency inside narrow limits. When the external reference returns, the oscillator will slowly correct for the accumulated drift in time, gently bringing the outputs back into perfect sync.
When the generator operates in flywheel mode, the flywheel inertia will gradually be exhausted and will eventually expire after a maximum of 20 seconds. If the incoming reference is not reestablished before this happens, control is handed over to the internal crystal reference. This scheme ensures continuous synchronization of the connected equipment, even when large dropouts of the incoming sync signal are to be expected. Further, the phase locked loop exhibits an excellent Jitter Rejection Ratio, and is able to clean up and stabilize a jittery house sync.
When more than one input source is connected, the generator automatically selects the active input by priority. 1: Video. 2: Word. 3: AES.
4: Internal crystal.

Powering up

There are no special considerations to observe when powering up the unit. When an external reference is connected upon power up, the generator will reset itself as close as possible to the relevant sync position, and it will immediately be able to achieve lock, as long as the incoming reference is better than +/-100 ppm in absolute frequency precision.

Video input

The Video input is not terminated internally; its impedance is 1 kohms. This makes it possible to connect the generator in a serial chain with other pieces of equipment, placing the correct 75 ohms termination at the end of the chain.
A jumper on the PCB provides an option to create a balanced input mode, useful when ground loops are present in the installation. The ground is lifted and connected to the inverting input of the input

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buffer, thus creating a balanced configuration with the screen of the input cable as the inverting input and the core as the non-inverting input.
Care should be taken not to exceed the Common Mode Range of the input circuit, which is 3.0 V.
The DSG3 will lock to standard interlaced PAL video with amplitudes ranging from 0.1 to 4.0V, 625 lines, 50 Hz vertical frequency and 15625 Hz horizontal frequency. The video signal must be interlaced, as the input sync separator extracts timing information from the odd/even video field information in the composite sync signal. Chrominance or 4.43 MHz subcarrier is not necessary.

Word input

The Word input is standard TTL compatible and unterminated. Its impedance is 10 kohm.

AES input

The AES input is transformer balanced, 110 ohms terminated as prescribed in the AES/EBU standards for professional/broadcast equipment.

Word output

There are two individually buffered Word outputs, 75 ohm, TTL level.

AES output

There are two individually buffered transformer balanced AES outputs, 110 ohms RS422 as prescribed in the AES/EBU standards for professional/broadcast equipment.

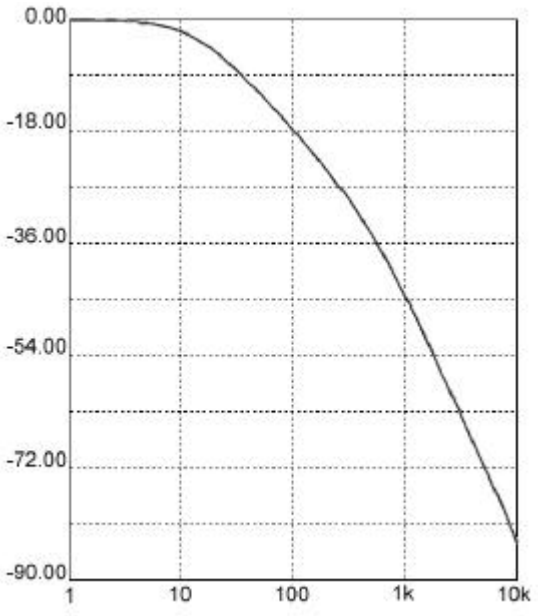
No Sync alarm

The alarm output is TTL level, 1 kohm. It is high when lock to external reference is established. It changes state to low when sync is lost.

Ability to reject jitter

The maximum permissible sample-to-sample jitter at the AES input is 45 nSec PP, equal or less than one half cycle of the master clock.

The Video and Word inputs are more tolerant, and they will accept and lock to input signals with up to 1 uSec jitter.
The jitter presented at the inputs will not directly be transferred to the outputs. It will be greatly reduced and in most situations almost total eliminated.
The curve illustrates the excellent Jitter Rejection Ratio of the DSG3. The corner frequency of the jitter rejection curve is approx. 12 Hz for the first pole and 500 Hz for the second pole. In the frequency band above 700 Hz, where excess jitter can create problems in standard A/D and D/A converters, the output jitter is reduced to residual HCMOS buffer noise, even with extreme jitter levels at the inputs.



Jitter Attenuation dB vs. Frequency.
AES input to AES output

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Additional Technical Information

General

The DSG3 has a straight forward, but powerful architecture. The input reference is automatically selected by priority from left to right on the front panel and fed to the sync input circuit. When a video input is present, the AES generator circuit locks the Z-preamble (at 48 and 96 kHz) or the X-preamble (at 44.1 kHz) to the video frame start. When an AES input is present, the generator locks the AES output Z-preamble to the AES input Z-preamble. Input word and output word is aligned edge to edge.
The internal flywheel is able to keep the outputs running at better than 0.5 ppm accuracy for up to 20 seconds, in case the incoming sync is momentarily absent.

Video input cct

The Video input circuit locks the input video frame to the output AES block by slowly changing the frequency of the crystal oscillator. The maximum time shift between input and output during the lock on sequence is ½ block, equal to 2 mSec. The lock time, when locking to a video signal, can amount to 40 seconds worst case.

Word input cct

The Word signal contains left/right information (X/Y preamble) so the generator simply locks the leading edge of the input word to the leading edge of the output word.
In order for this to happen, the input and output sampling rates must be identical.
The lock time is approximately 3 seconds with a maximum time shift during the lock on sequence of ½ word, equal to approx. 10 uSec.

AES input cct

The AES input signal is aligned to the AES output signal, by comparing the input Z-preamble to the output Z-preamble, thus in effect creating an output identical to the input.
However, only block position and frequency are mirrored. The generator ignores the audio data and channel status of the input, substituting these with its own data and channel status information.
The maximum time shift between input and output during the lock on sequence is ½ block, equal to 2 mSec.
The lock time when locking to an AES signal can amount to 40 seconds worst case.

Flywheel cct

When the input is lost, an internal flywheel circuit immediately takes over, keeping both clock frequency and position of the preambles inside narrow limits. When the input returns, the generator slowly corrects for the accumulated drift in time, gently bringing the preambles back into perfect sync.
When operating in flywheel mode, the flywheel inertia will gradually be exhausted and it will eventually expire after a maximum of 20 seconds. If the input is not reestablished before timeout, clock control is handed over to the internal crystal reference. Operation of the flywheel circuit is identical in all input modes.

AES Outputs

The AES outputs are available on the SUB-D connector on the back panel. The outputs are individually buffered, 110 ohms, transformer balanced and 4V PP when terminated.
The AES signal is intended for synchronization purposes and should normally be empty of audio data, i.e. all audio data bits are set to zero. This would minimize the build-up of jitter in cables, as the format produces a biphase coded AES signal with a large portion of the frame having identical pulses.
However, some commercially available AES receiver chips exhibits PLL lock problems when subjected to a "black" AES signal, producing an unstable and jittery master clock.
The problem has been overcome by setting the first eight audio data bits to 1 and the remaining sixteen bits to 0. This gives a DC offset in the

audio signal of –90 dBFS or approximately 0.2 mV with reference to +18 dBu.
A standard digital audio input circuit will easily accommodate this DC offset, and the scheme efficiently eliminates the AES receiver lock problems.

44.1kHz/48kHz/96 kHz sampling frequency

The AES/Word generator output sampling frequency is selected by a pushbutton that toggles between the available frequencies. The pushbutton has a 2 seconds time delay to protect against accidental change.
Default start up sampling frequency can be set by internal wiring to 44.1 kHz, 48 kHz or 96 kHz.

Word Outputs

The Word outputs are available on the standard SUB-D connector on the back panel. The outputs are individually buffered, 75 ohms and TTL level. The word output frequency follows the chosen sampling frequency on the front panel, i.e. 44,1 kHz, 48 kHz or 96 kHz.

The rising edge of the word is aligned to the AES subframe A and the trailing edge is aligned to the AES subframe B. Thus a high level indicates left channel and a low level indicates right channel of the audio data.

GPU Bus outputs

The Generator outputs all relevant clocks and control signals on a 10-bit GPU bus connecting all modules in the GPU frame.
The signals are used to control and synchronize digital output modules, such as Analog/Digital and Sample Rate Converters, in order to ensure correct synchronization of all digital outputs.
The GPU bus also performs reset requests, Out Of Sync monitoring and direct communication with the BBG3 Video Generator and the WDIS8 and ADIS8 distribution amplifiers.

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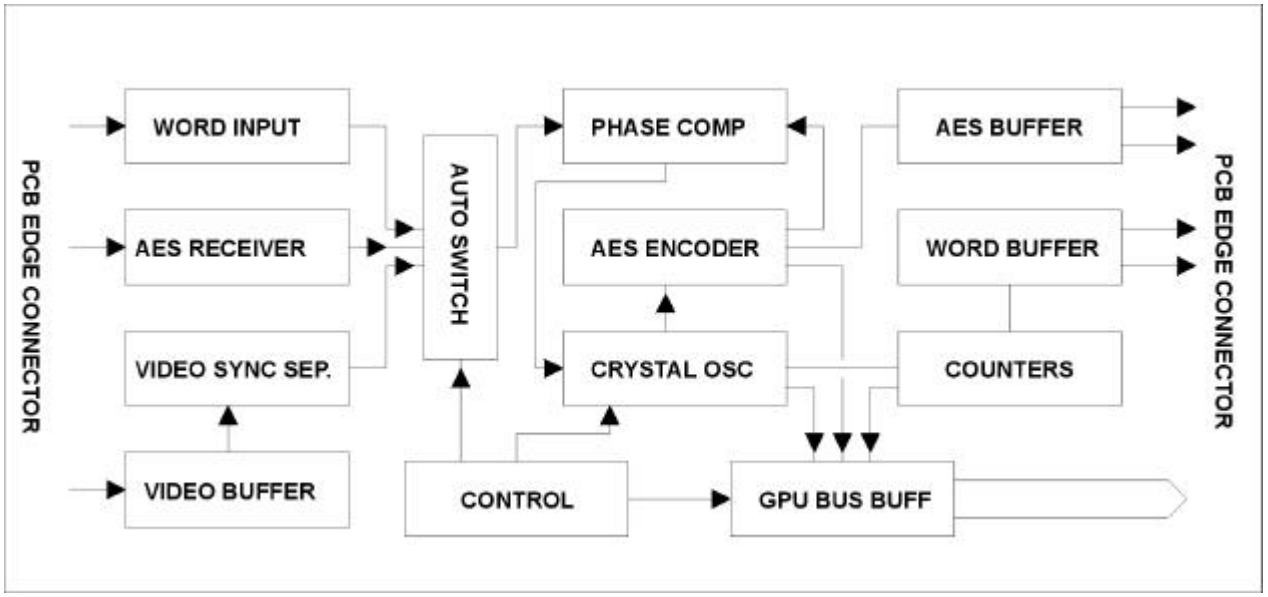
Block Schematic:



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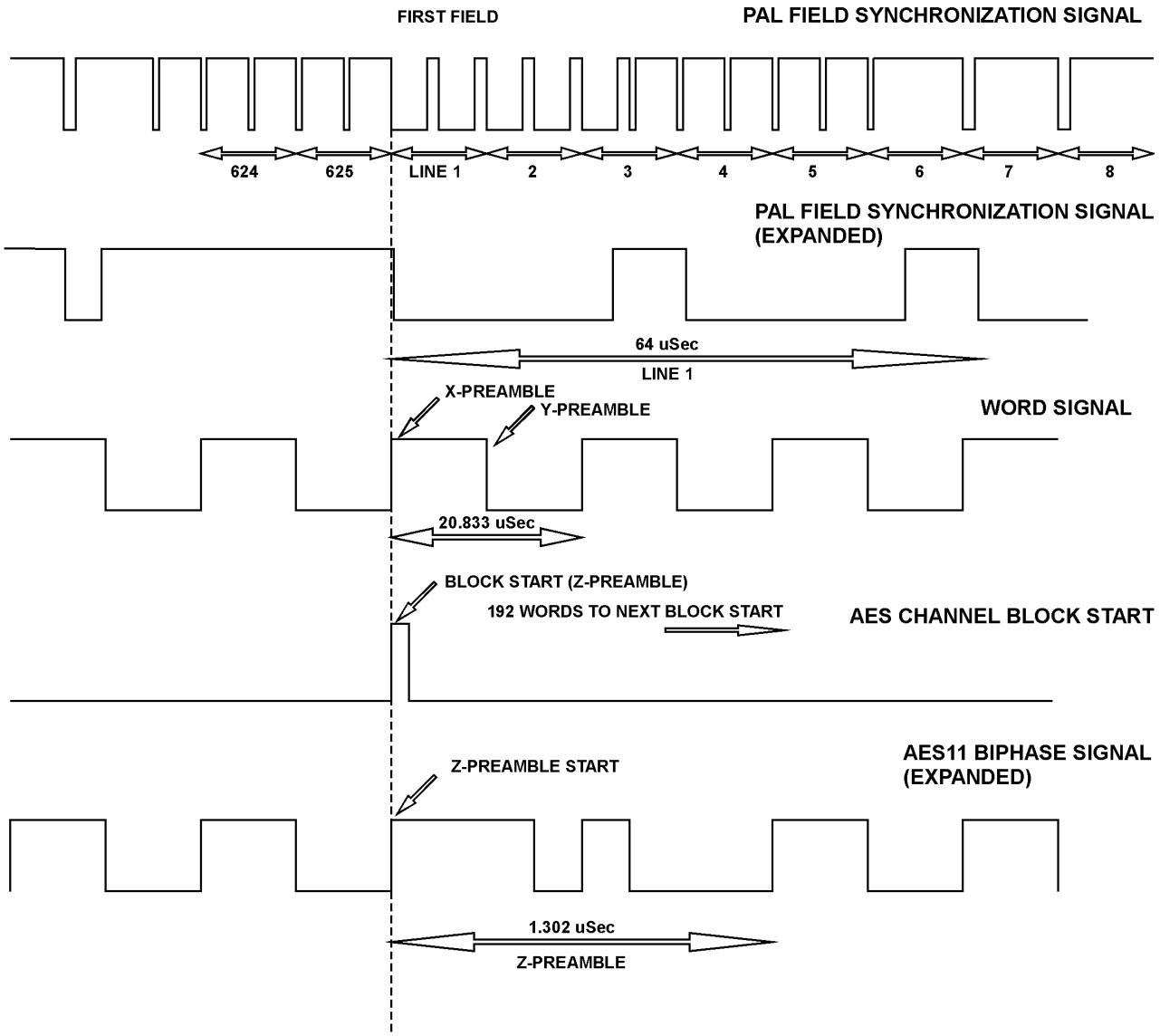
Relationship between Video, Word and AES



The generator places the video, word and AES block start as seen on the graphic representation above.
At 48 kHz sampling frequency, the relationship is straightforward:
1 Video field = 5 channel blocks = 960 words. 1 channel block = 192 words
At 96 kHz sampling frequency, the relationship is also straightforward:
1 Video field = 10 channel blocks = 1920 words.1 channel block = 192 words
At 44.1 kHz sampling frequency, the relationship is less useful:
1 video field = 882 words. But the AES block is still 192 words, so no simple defined position of the AES block start in the video field is possible. This is the reason the generator switches to word mode at 44.1 kHz sampling frequency.

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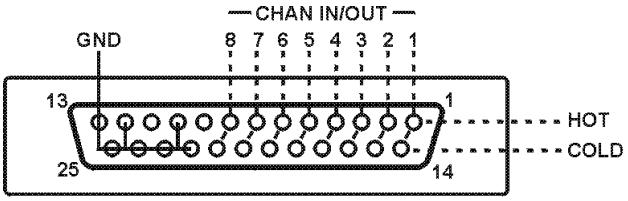
Electrical specifications:

Reference Inputs : Composite PAL Video, balanced 1kohm, 0,1 -4,0V PP
: AES balanced 110 ohms RS422
: SDIF-2 word clock, 10 kohms, TTL level

Outputs : 2 x AES11 transformer balanced 110 ohms RS422
: 2 x SDIF-2 word clock, 75 ohm, TTL level
: No-sync alarm 1 kohm TTL level

Stability/accuracy : Crystal accuracy 5 ppm/25 deg. C, stability 0.2 ppm/ deg. C
: PLL capture range max. +/-100 ppm.
: PLL jitter < 1,5 nsec SS, 700Hz - 100kHz

IN/OUT CONNECTIONS DSG3



Video Input: Hot pin1, Cold pin14
Word Input: Hot pin2, Gnd pin15
AES Input: Hot pin3, Cold pin16, Gnd pin17
No Sync alarm: Hot pin4, Gnd pin17
Word Output 1: Hot pin5, Gnd pin18
Word Output 2: Hot pin6, Gnd pin19
AES Output 1: Hot pin7, Cold pin20, Gnd pin22
AES Output 2: Hot pin8, Cold pin21, Gnd pin 23

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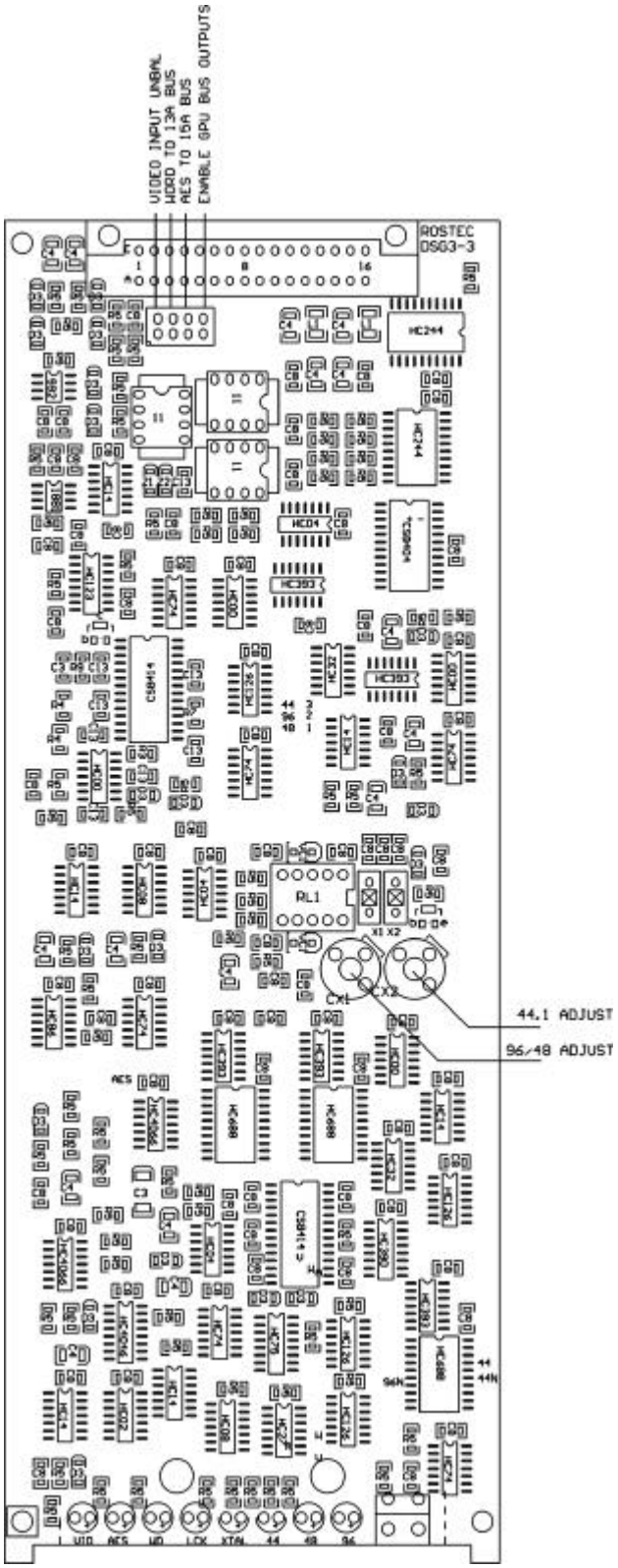

Jumper settings:
Video jumper on: Unbalanced mode (default)
Video jumper off: Balanced mode

Word jumper on: Word to bus enabled
Word jumper off: Word to bus disabled (default)

AES jumper on: AES to bus enabled
AES jumper off: AES to bus disabled (default)

GPU jumper on: GPU timing enabled (default)
GPU jumper off: GPU timing disabled