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ROSTEC T535E, 2Mbit/E1 G.703 TRANSMITTER INTERFACE for GPU frame

General description

The T535E Transmitter Interface is designed to operate in the GPU frame as an extension to the DSG3 or DSG5E Reference Generators, extracting all the necessary clocks and references from the GPU bus. It is, however, able to operate on its own, with or without other modules installed in the frame, if an external 2.048 MHz reference clock is applied.
It outputs a 2Mbit E1 ITU-T G703/704 compliant reference signal and a 2.048 MHz reference clock at TTL level. The Line Interface supports AMI or HDB3 line encoding, and the framer supports unframed G703 (all ones mode), basic G704 framing and G704 CRC-4 multiframe mode.

Both the E1 and the 2.048 MHz signals are generated by an on board crystal controlled oscillator, phase locked to the GPU bus or to an incoming 2.048 MHz clock.
The operation of the T535E does not depend on the selected AES sampling frequency on the reference generators. It locks to the 44.1 kHz, 48 kHz and 96 KHz AES sampling frequency via the GPU bus, keeping the correct mathematical relationship between Fs and the generated E1 signals.
Note that there exists no simple positional relationship between E1 signals and AES/word signals. The T535E calculates the frequency relationship and performs a phase lock based on the common denominator of the signals.
The common denominator is available at a test point on the PCB board for scope triggering during service or test procedures.

2Mbit E1 G.703/704 outputs

The T535E also works as a distribution module, having four 2.048 MHz outputs and four E1 G703/704 outputs.
The four E1 outputs are individually buffered and transformer balanced, having the transformer center-grounded at the IC side and floating at the line output side. The output pulse shape meets the ITU G.703 Pulse Mask template for 75 Ohms coaxial cable load.

2.048 MHz output

The four 2.048 MHz outputs are individually buffered, single ended TTL compatible and 75 Ohms impedance.

Lock/Error LED

The LOCK LED on the front should always be lit under normal operating condition. It indicates, that the phase lock, and thus the correct relationship between E1 and AES/Word, exists.
The ERROR LED will light up momentarily when the GPU frame is powered up, but will normally be extinguished.
It will light up briefly when sampling frequency is changed on the DSG3 or the DSG5E, and it *may* light up while the DSG3 or the DSG5E is

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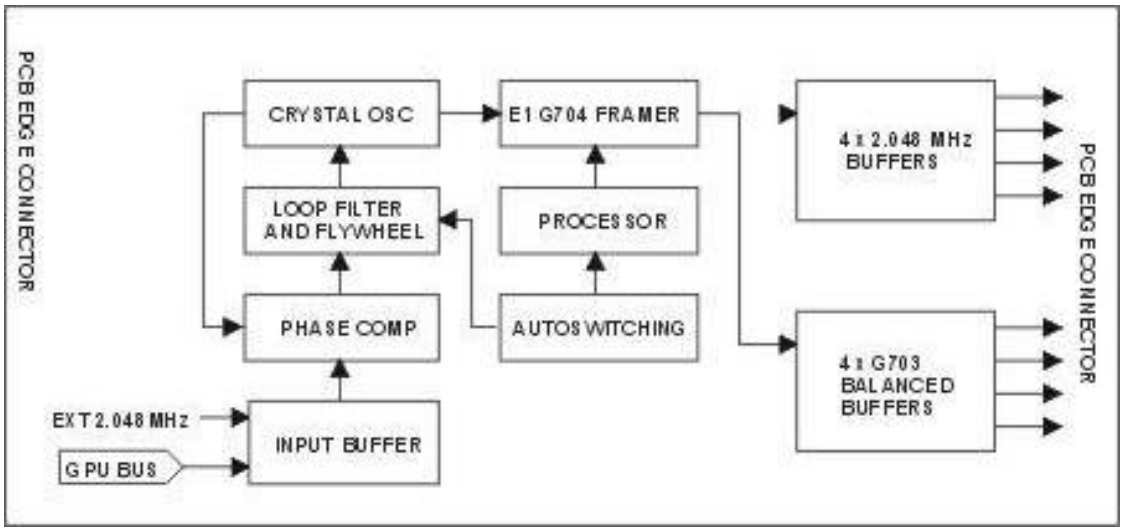
searching for lock or performing its lock-on sequence. The two LEDs can be considered as status indicators.

Block schematic



Electrical specifications:

Reference Inputs : GPU Bus signals from DSG3/DSG5E Reference Generator
: External 2.048 MHz clock, TTL compatible

Outputs : 4 x E1 ITU G.703 compliant, Transformer balanced 75 Ohm, compliant to ETSI 300 166 Return Loss Requirement
: 4 x 2.048 MHz clock, 75 ohm, TTL level
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Stability/accuracy : Identical to reference source, DSG3/DSG5E or external 2.048 MHz
: PLL capture range max. +/-50 ppm.
: PLL jitter < 1 nSec 700Hz - 100kHz

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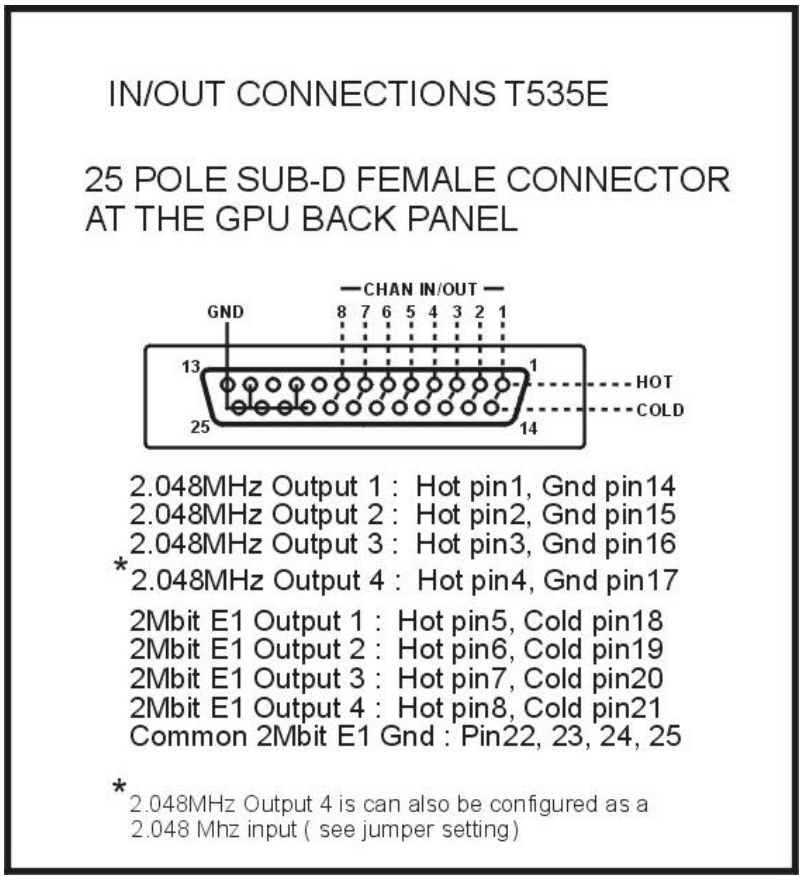
Input output connections



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Jumper settings

General description

The user can select some of the most common frame/data options in the G704 format by setting jumpers on the PCB.
Only the various formats that are relevant to synchronization have been assigned to the jumpers.

Input/Output Config.

2M OUT: Normal configuration, i.e. 4 x 2.048 MHz outputs and 4 x G.704 E1 outputs.

2M IN: The 2.048 MHz output no.4 is configured to be an input, used to synchronize the 535E to an external 2.048 MHz clock. (Pin 4 is hot and pin 17 is ground on the backplane SUB-D connector).

AUTOREF: A jumper placed here enables the automatic switching between references.
When no external signal is applied, the GPU frame bus is the reference (DSG5E, DSG3).
When an external 2.048 MHz input is applied (pin4/17), the circuit automatically selects it as a reference and locks on to it. When the external input is lost, the circuit immediately switches back to the GPU frame reference generator.
When no jumper is placed in this position, the T535E waits for an external input. Any reference generator in the GPU frame will be ignored.

Output Control

NORM: All outputs are permanently on.

PLL: The outputs are muted when the T535E is out of lock. This option is useful, when using the T535E with an external 2.048 MHz as the only reference.
With no reference available, the on-board crystal generator will continue at an arbitrary frequency defined only by the limits of its capture range, i.e. +/- 50 ppm. *Setting the jumper to PLL will ensure that only when the conversion from 2.048 MHz to G704 is precise, the signals will be presented at the outputs.*

G704 Frame Format Config.

The jumpers are labeled 0 – 7 as seen from the front of the PCB.

Jumper 0: This jumper is for debugging.
A jumper placed in this position enables the micro controller program to repeat continuously (default)
No jumper in this position makes the program run once after a reset, and then stop.

Jumper 1: This jumper selects the transmitter line encoding scheme
A jumper placed in this position selects AMI encoding (default).
No jumper in this position selects HDB3 encoding.

Jumper 2: This jumper selects the Channel Associated Signaling multiframe alignment (CAS)
A jumper placed in this position enables CAS (default)
No jumper placed in this position disables CAS and the framer defaults to basic frame alignment.

Jumper 3: This jumper selects idle code.
A jumper placed in this position forces all channels into a trunk condition state with idle code substitution and signaling substitution.
No jumper placed in this position enables normal operation (default).

Jumper 4: This jumper selects G703 or G704 format.
A jumper placed in this position will force the transmitter to ignore any framing command and generate an unframed All Ones signal at the output. The jumper is a master override.
No jumper placed in this position will enable the G704 framing as selected by the other jumpers (default).

G704 Frame Data Config

This group of jumpers is labeled CAS DATA 1-4 and PCM DATA 1-2. They control the contents of the frames rather than the actual frames format. The setting of these jumpers is ignored when jumper 4 is on (G703 All Ones selected)
The purpose of the jumpers is to insert signals into the frames, creating a signal that is easy for the receiver to lock on to.
Many commercial receivers exhibit difficulties in locking on to a string of empty frames, even when the frame format and frame boundaries are correctly defined. The signals inserted by these

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jumpers are without meaning to the receiver. They only serve as a basis for a reliable clock extraction.

CAS DATA 1-4 inserts a fake address into the Channel Signaling Bits position.
CAS DATA 1 sets the address to 0101 (default)
CAS DATA 2 sets the address to 0011
CAS DATA 3 sets the address to 0000
CAS DATA 4 sets the address to 1111

PCM DATA 1-2 inserts a dummy signal into the PCM data in the frames.
PCM DATA 1 inserts 8 ones and 8 zeros repeatedly (default)
PCM DATA 2 inserts 16 ones and 16 zeros repeatedly.

Programming Port

These pins are not for jumpers. They are a port for an external programmer, used to interface with and program the microcontroller. **Do not place any jumpers here.**

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Jumpers on the PCB Board: